Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): An error detection and correction circuit for detecting and correcting an error in an input signal containing a first signal and a second signal, comprising:

a signal separation circuit for receiving the input signal and extracting the first signal and the second signal from the received signal, the signal separation circuit providing a switching signal;

a selection circuit for selecting either the first signal or the second signal in the input signal to an error detection and correction unit depending on the switching signal input signal, the selected first signal or second signal providing an input to an error detection and correction unit;

an error detection and correction unit for detecting and correcting an error in an output signal from the selection circuit;

a switch circuit for receiving a switching signal from the signal separation circuit for outputting an output signal from the error detection and correction unit to either an output path for the first signal or an output path for the second signal; and

a memory;

and wherein the ~~selection~~ signal separation circuit ~~selects~~ separates the second signal from the input signal and sends the second signal to the memory;

the memory stores the second signal until an amount of the stored second signal becomes a predetermined amount; and

the error detection and correction unit receives the predetermined amount of the second signal where the amount of the second signal in the memory becomes the predetermined amount.

2. (Previously Presented): An error detection and correction device according to claim 1, wherein

the error detection and correction unit includes the memory, and the memory stores the first signal and the second signal.

3. (Original): An error detection and correction device according to claim 2, wherein the memory has a first predetermined area storing the first signal and a second predetermined area storing the second signal.

4. (Previously Presented): An error detection and correction device according to claim 1, wherein

the error detection and correction unit receives the first signal when the first signal is supplied, and conducts error correction to the first signal received, and

the error detection and correction unit receives the second signal when the second signal is supplied, and conducts error correction to the second signal received.

5. (Original): An error detection and correction device according to claim 1, wherein the first signal occupies a larger portion of the input signal than the second signal.

6. (Original): An error detection and correction device according to claim 1, wherein the first signal is a main signal and the second signal is a TMCC signal,

and wherein both are present in a received signal for satellite digital television broadcasting.

7. (Currently Amended): An error detection and correction circuit for detecting and correcting an error in an input signal containing a first signal and a second signal, comprising:

a signal separation circuit for receiving the input signal and extracting the first signal and the second signal from the received signal, the signal separation circuit providing a switching signal,

a selection circuit for selecting either the first signal or the second signal in the input signal to an error detection and correction unit depending on the switching signal input signal, the selected first signal or second signal providing an input to an error detection and correction unit;

an error detection and correction unit for detecting and correcting an error in an output signal from the selection circuit; and

a switch circuit for receiving a switching signal from the signal separation circuit for outputting an output signal from the error detection and correction unit to either an output path for the first signal or an output path for the second signal; wherein

the error detection and correction signal sets a completion flag upon completion of error detection and correction with respect to the first signal received, and

the ~~selection~~ signal separation circuit supplies the second signal to the ~~error detection and correction unit~~ selection circuit when the ~~selection~~ signal separation circuit receives the second signal and detects the completion flag.

8. (Original): An error detection and correction device according to claim 7, wherein

the error detection and correction unit calculates a syndrome based on the input signal, processes the syndrome calculated to calculate an error position polynomial and an erroneous value polynomial, and conducts error correction based on the error position polynomial calculated and the erroneous value polynomial calculated, and

the error detection and correction unit sets the completion flag upon completion of calculation of an error position polynomial and an erroneous value polynomial with respect to the first signal.

9. (Original): An error detection and correction device according to claim 7, wherein the first signal occupies a larger portion of the input signal than does the second signal.

10. (Currently Amended): An error detection and correction device according to claim 9, wherein the ~~selection~~ signal separation circuit supplies the second signal to the ~~error detection and correction unit~~ signal selection circuit when the ~~selection~~ signal separation circuit receives a predetermined number of second signals and detects the completion flag set.

11. (Original): An error detection and correction device according to claim 9, wherein the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.